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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,308	04/28/2004	Hsiang-An Hsieh	12221-US-PA	3307

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
VO, THANH DUC	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,308	HSIEH, HSIANG-AN	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the Application filed on April 28, 2004. Claims 1-11 are presented for examination. Claims 1-11 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

A processor 140 on page 2, paragraph 0006, line 8 should be written as – a processor **114**.

Appropriate correction is required.

Claim Objections

3. Claims 1-11 are objected to because of the following informalities:

(a) "topre-store" should be written as – and pre-stores (claim 1).

(b) the phrase "topre-store a portion of the data therein which are other of said data required by the read signal" should be written as – and pre-stores a portion of the plurality of data therein other than data required by the read signal (claim 1).

(c) "intosaid cache" should be written as – into said cache (claim 2, page 2).

(d) "said operative signal" should be written as – said operation signal (claim 2).

(e) "to store" in line 14 of claim 2 should be written as – "and stores".

(f) "saidcache" should be written as – said cache (claim 2, page 2).

(g) "a data" should be written as – data (claim 2, page 2, line 3-4).

(h) "conform" should be written as – conforms (claim 2, page 2).

(i) "alternately synchronously" should be written as – alternately and synchronously (claims 4 and 8).

(j) "receiving a first data" should be written as – receiving first data (claim 5).

(k) "storing a second data" should be written as – receiving second data (claim 5)

(l) the phrase "conform to a third data required requested by" in line 12 of claim 5 should be written as – conforms to third data required by.

(m) the term "conform" in claim 6 should be written as – conform.

(n) "intosaid cache" should be written as – into said cache (claim 5, page 2).

(o) "tosaid third" should be written as – to said third (claim 6, page 3).

(p) "and a write data" in line 3 of claim 9 should be written as – " and write data"

(q) "said write data signal in line 5 of claim 10 should be written as – said write data.

All dependent claims are objected to as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1-4 rejected under 35 U.S.C. 102(e) as being unpatentable by Kadi (US 2004/0117556).

As per claims 1 and 2, Kadi discloses a controller of a silicon storage apparatus, comprising:

a processor (Fig. 2, processor);

a system interface (Fig. 5, item 30), adapted for receiving an operation signal;

a memory interface (see Fig. 5, item 45) wherein a bus inherently comprising an interface that is coupling to the solid-state storage medium;

a solid-state storage medium (Fig. 5, item 50, nonvolatile memory), adapted for storing a plurality of data;

a transmission buffer (Fig. 2, item 202), coupled to said memory interface and said system interface;

a cache buffer (Fig. 2, item 204), overlapping said transmission buffer (Fig. 2, item 202) to couple to said memory interface and said system interface;

wherein when said operation signal is a read signal, said processor retrieves an address mapping table (*Fig. 4B, the address column of pre-fetched data, which is equivalent to the address mapping table since the address is corresponded with a data*) to store a pre-storage data which is not indicated by said read signal into said cache buffer (*page 3, paragraph 0032, lines 10-15, wherein the data is pre-fetched and stored in the pre-fetch buffer/cache buffer*); and

when said operation signal is a subsequent read signal, said cache buffer stores

a data, and said processor determines whether or not said data conform to said pre-storage data (see page 4, claim 11, lines 5-8).

As per claim 3, Kadi discloses an allocation table buffer area (Fig. 4A, Address buffer), coupling to said system interface and said memory interface, adapted to store said address mapping table (page 3, paragraph 0032, lines 1-2).

As per claim 4, Kadi discloses a controller of a silicon storage apparatus as cited in claim 2, wherein said cache buffer and said transmission buffer alternately and synchronously transmit data. See page 4, claim 11, lines 5-8 and claim 13. *The pre-fetch buffer and the transaction buffer are alternating each other and synchronously (occurring at real-time) transmitting the data.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 8, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadi (US 2004/0117556) in view of Pettey et al. (US 6,055,590).

As per claim 5, Kadi disclosed a data transmission method of a controller of a silicon storage apparatus, said silicon storage apparatus comprising:

a system interface (Fig. 5, item 30), adapted for receiving an operation signal;

a memory interface (see Fig. 5, item 45) wherein a bus inherently comprising an interface that is coupling to the solid-state storage medium;

a transmission buffer (Fig. 2, item 202), a cache buffer (Fig. 2, item 204), an allocation table buffer area (Fig. 4A, Address Buffer), said method comprising:

receiving a first data required by a read signal by said transmission buffer (page 3, paragraph 0028, lines 13-14);

storing a second data not indicated by the read signal into said cache buffer (page 3, paragraph 0032, lines 10-15); and

comparing and determining whether said second data conform to a third data required requested by a subsequent read signal (page 4, claim 11, lines 5-8).

Kadi did not specifically disclose a method where storing a second data not indicated by the read signal into said cache buffer **after the transmission buffer being saturated** (emphasis added). However, Pettey et al. disclosed a method wherein the transaction (such as read) is overflow into another buffer when the last unused buffer is full/saturated (col. 16, lines 17-20). It would have been obvious to one having an ordinary skill in the art at the time of the applicant's invention to modify the system of Kadi to combine the method taught by Pettey et al. in order to arrive at the current invention while improving the efficiency of the system because all of the data to

be transferred can be transferred before the transaction is terminated as taught by Pettey et al. on col. 2, lines 4-10.

As per claim 8, Kadi disclosed a data transmission method of a controller of a silicon storage apparatus as cited in claim 5,

wherein the cache buffer and the transmission buffer alternately synchronously transmit data. See page 4, claim 11, lines 5-8 and claim 13. *The pre-fetch buffer and the transaction buffer are alternating each other and synchronously (occurring at real-time) transmitting the data.*

As per claim 9, Kadi disclosed a data transmission method of a controller of a silicon storage apparatus as cited in claim 5,

wherein when said system interface receives a read signal and a read data in response thereto, said processor reads said read data into a solid-state medium according to a address mapping table (See Fig. 4A-4B with respect to the Flash memory, Address Buffer/mapping table, the pre-fetched data with address); and

when the process for reading data is completed, said address mapping table is written into said solid-state medium (Fig. 4B, wherein the address of the Flash memory is corresponded to the address in the Address Buffer).

Although Kadi was not specifically disclosing the step of storing/writing a data into a solid-state medium but it would have been readily apparent to one having an ordinary skill in the art at the time of the applicant's invention to realize that the data

has to be written into the solid-state medium/flash with the same manner so that the data and the address are corresponded with each other in order to avoid any data redundancy or the address being pointed to wrong data.

As per claim 11, Kadi disclosed a data transmission method of a controller of a silicon storage apparatus,

wherein the content of said address mapping table is renewed according to the transmission of said write signal (See Fig. 4B, wherein data, address buffer/table, and pre-fetched data are previously stored and renewed accordingly);

said processor writes said write data into said solid-state storage medium from said cache buffer through said memory interface (See Fig. 4B, wherein the data in the Flash is being written from memory interface accordingly by using the address buffer and the cache buffer which comprises of pre-fetched data and the address); and

when the process of said writing is completed, said address mapping table is written into said solid-state medium (See Fig. 4B, wherein the address in the Flash is corresponded to the address in the Address Buffer (0x70000020)).

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadi (US 2004/0117556) and Pettey et al. (US 6,055,590), and further in view of Dover et al. (US 2003/0204675).

As per claim 6, Kadi discloses a data transmission method of a controller of a silicon storage apparatus, wherein the step of determining whether said second data conform to said third data required by said subsequent read signal, further comprises:

outputting said second data from said cache buffer when said second data conform to said third data (page 4, claim 11, lines 5-8); and

Kadi or Petty et al. did not specifically disclose a method of removing the second data from the cache buffer when the second data does not conform to the third data.

Dover et al. disclosed a method of removing the second data from the cache buffer when the second data does not conform to the third data (Fig. 2, item 260).

It would have been obvious to one having an ordinary skill in the art at the time of the applicant's invention to recognize that it is advantageous to combine the method of Dover et al. with the method of Kadi in order to arrive at the current invention since removing the miss-hit data from the cache will enable the cache buffer to store the higher read frequency data into the vacant location of the cache buffer to improve the data throughput.

As per claim 7, Kadi or Petty et al. did not disclose a data transmission method of a controller of a silicon storage apparatus, wherein the cache buffer comprises at least one minimum accessing unit, and said minimum accessing unit comprises at least one sector. However, Dover et al. disclosed a cache memory and a collection of data (collection of data equivalent to cluster, wherein cluster is one form of minimum accessing unit that is defined by Applicant in paragraph 0027 of the Specification), and

said minimum accessing unit comprises at least one sector (page 1, paragraph 12, lines 2-5). It would have been obvious to one having an ordinary skill in the art at the time of the applicant's invention to readily recognize that a cluster a collection of data comprising one or more sectors in a storage medium. Therefore, it would have been obvious to one having an ordinary skill in the art to store data as a cluster in a storage medium since a cluster is the smallest unit of disk space that can be allocated for use by files.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadi (US 2004/0117556), Pettey et al. (US 6,055,590) and further in view of Williams et al. (US 6,976,128).

As per claim 10, Kadi or Pettey et al. did not specifically disclose all limitation of a data transmission method of a controller of a silicon storage apparatus,

wherein said cache buffer receives said write data transmitted from said system interface while said processor is decoding said write data signal; and

when the process of said decoding is completed, said write data is written into said solid-state medium from said cache buffer through said memory interface.

However, Williams et al. discloses a cache buffer (cache memory), system interface (primary interface), a decoder in processor (decode circuit), solid-state medium (main memory), and memory interface (background interface), wherein the cache buffer receives a write data transmitted from the system interface while the

processor is decoding a write data signal; and when the write data signal is decoded the write data is written/flush into the solid-state medium from the cache buffer through the memory interface. See claim col. 18, claim 43, its entirely. It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Williams et al. with the method of Kadi and Pettey et al. to arrive at the current invention. The motivation of doing so is to ensure that the processor uses the same copy of data by periodically be flushed to the main memory as new data is stored within the cache memory as taught by Williams et al. on col. 1, lines 32-35.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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4/10/2006

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